Objection to the Specification

The Examiner objects to the specification as allegedly failing to provide proper antecedent basis for the feature "portions of the second impurity regions" of claim 18. Applicant respectfully contends that sufficient antecedent basis exists throughout the Applicant's specification for "portion of the second impurity regions." For instance, claim 18 requires a gate electrode which overlaps the first low concentration impurity regions and portions of the second impurity regions. Page 9, lines 7-10 recites that the LDD region ("lightly doped region") 111a and the LDD region 111d have a region that overlaps with a gate electrode and a region that does not. See, Figure 1. Moreover, page 19 of the specification describes that "the LDD regions 236a, 236b are formed so as to partially overlap with the gate electrode 226." See, Figure 4A. It is contended that both of these passages at least implies that the gate electrode overlaps a portion of the impurity regions. Accordingly, reconsideration and withdrawal of the objection is earnestly solicited.

B. 35 U.S.C. §103 Rejection

The Examiner rejects claims 1, 2, 21 and 22 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,323,042 to ***Matsumoto*** in view of U.S. Patent No. 5,528,056 to ***Shimada et al.*** (Hereinafter "***Shimada***"). Applicant respectfully traverses this rejection for at least the reasons advanced hereinbelow.

The claimed invention is directed generally to a display device comprising a pixel portion and a driver circuit portion on a substrate, the pixel portion including, *inter alia*, a semiconductor film comprising a plurality of channel forming regions, a plurality of impurity regions, a source region, and a drain region, and a gate electrode overlapping with the channel forming regions and some of the impurity regions, with a gate insulating film interposed therebetween.

Applicant respectfully contends that the claimed invention defines subject matter which is clearly patentably distinct over the prior art. More particularly, it is contended that the ***Matsumoto*** patent, either alone or in combination with the ***Shimada*** patent, fails to expressly teach or implicitly suggest each and every limitation of the claimed invention necessary to support a finding of *prima facie* obviousness under 35 U.S.C. §103(a).

For instance, in the Office Action, the Examiner finds that the ***Matsumoto*** patent discloses a display device having a pixel portion 12 comprising a semiconductor film comprising a channel region 21a, "a plurality of impurity regions 21b," and source and drain regions 21c, and "a gate electrode 25 overlapping/partially overlapping with the channel region 21 a and some of the impurity regions 21 a, b, with a gate insulating film 24 interposed therebetween." Thus, the Examiner concedes that the ***Matsumoto*** patent is deficient for failing to disclose a plurality of channel regions and a plurality of impurity regions. The ***Shimada*** patent is thereby cited by the Examiner to show a semiconductor film having two channel regions with an impurity region interposed between the channel regions.

However, a proper reading of the disclosure of the ***Shimada*** patent clearly shows that it fails to modify the ***Matsumoto*** patent in a manner sufficient to render the claimed invention obvious. What the ***Shimada*** patent in fact discloses is <u>two</u> gate electrodes 7a and 7b formed over two channel regions 16a and 16b, respectively, and <u>one</u> impurity region 29 located between the two channel regions 16a and 16b. Thus, the ***Shimada*** patent fails to either expressly, implicitly or inherently disclose a gate electrode overlapping with a plurality of channel regions and some impurity regions, and said some impurity regions located between the channel regions and under the gate electrode.

On the other hand, the claimed invention requires <u>a plurality of impurity regions</u>, a source region, and a drain region, and <u>a single gate electrode</u> overlapping with some of

the impurity regions, with a gate insulating film interposed therebetween. See, FIGs. 1, 4A, 6D, and 9 of the subject application. There is no mention throughout the disclosure of ***Shimada*** of an embodiment which encompasses the aforementioned combination.

Therefore, it is contended that the ***Matsumoto-Shimada*** combination is improper since the ***Shimada*** patent fails to disclose a combination of a plurality of impurity regions, a source region, and a drain region, and a single gate electrode overlapping with some of the impurity regions, with a gate insulating film interposed therebetween. Inasmuch as the ***Shimada*** patent fails to disclose these features of the claimed invention, *prima facie* obviousness cannot result from its combination with the ***Matsumoto*** patent. Accordingly, reconsideration of the pending claims and withdrawal of the rejection are respectfully solicited.

Conclusion

Prompt and favorable consideration is requested. In view of the above-noted arguments, the pending claims are believed to be in condition for allowance. Should the Examiner deem that any further action by the Applicant would be desirable in placing this application in even better condition for allowance, he is requested to contact the undersigned.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285
NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110
(703) 883-0370 FAX